CMOS Analog Integrated Circuit Design

Lecture 9: Bandgap Voltage References & SC Circuits

Reading: Razavi, Chs. 11, 12, Johns, Chs. 7, 14

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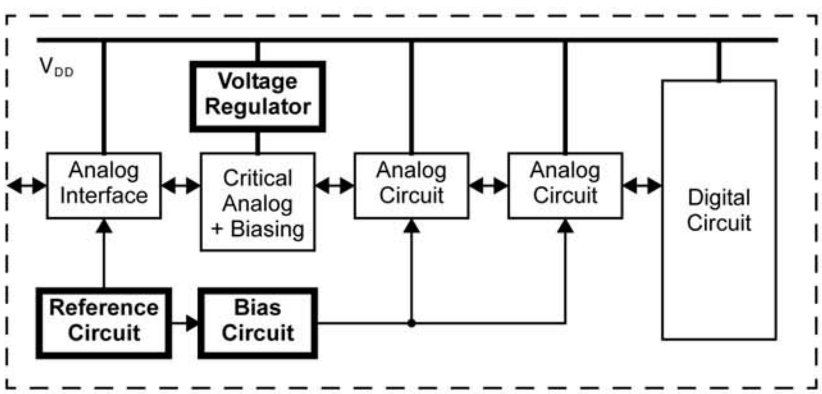
Applications

- Bias currents and voltages in analog circuits: mirrors, diff pairs, common-mode levels, etc.
- Reference voltage or current in A/D and D/A converters.



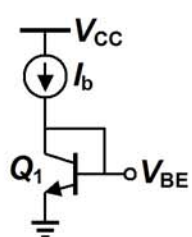
Basic Idea

- The main goal is to establish a dc voltage that is independent of the supply voltage, process parameters, and the temperature variations.
- Use a Zener diode breakdown voltage: it is beyond the supply voltage.
- Difference between threshold voltages of an enhancement and a depletion MOSFETs => depletion devices are not available.
- Combine two phenomena that vary with T in opposite directions, e.g., add two voltages with positive and negative TCs, such that the sum has zero TC.
- The dependence on temperature assumes one of two forms:
  - Proportioned to absolute temperature (PTAT)
  - Contrary to absolute temperature (CTAT)

$$V_{Ref} = \alpha_1 V_1 + \alpha_2 V_2 \quad \Rightarrow \quad \frac{\partial V_{Ref}}{\partial T} = \alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} = 0$$

Zero temp coefficient

CTAT Voltage Generation



$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$
$$V_T = kT/q$$

$$I_S \propto \mu k T\, n_i^2, \quad \mu \propto \mu_0 T^{\,m=-3/2}$$
$$n_i^2 \propto T^3 \exp\left(-\frac{E_g}{kT}\right)$$

$$\Rightarrow \quad I_S \propto T^{4+m} \exp\left(-\frac{E_g}{kT}\right)$$

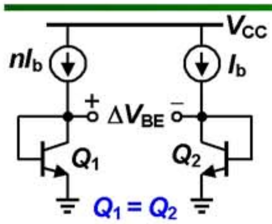
$$V_{BE} = V_T \ln\frac{I_C}{I_S} \quad \Rightarrow \quad \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

$$\Rightarrow \quad \frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

$$V_{BE} \approx 750\,mV \;\Rightarrow\; \frac{\partial V_{BE}}{\partial T} @ T = 300°K \approx -1.5\,mV/°K$$ ***An example***

- The base-emitter voltage of a forward biased diode-connected BJT with a fixed collector current has a negative TC. => **CTAT generator**
- TC of V_{BE} is temperature dependent => needing a variable PTAT generator.

PTAT Voltage Generation



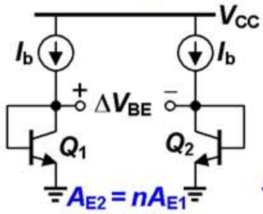
$$\Delta V_{BE} = V_T \ln\frac{I_{C1}}{I_{S1}} - V_T \ln\frac{I_{C2}}{I_{S2}}$$

$$I_{S1} = I_{S2}$$

$$\Rightarrow \Delta V_{BE} = V_T \ln n$$

$$\Rightarrow \frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q}\ln n > 0$$

Independent on temp



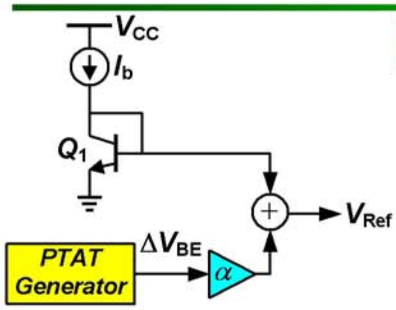
$$\Rightarrow \Delta V_{BE} = V_T \ln\frac{I_{C1}}{I_{S1}} - V_T \ln\frac{I_{C2}}{I_{S2}} = V_T \ln n$$

$$I_{S2} = nI_{S1}$$

Same bias currents with ratioed base-emitter junction areas

- Two identical transistors biased with different currents.
- The difference between the base-emitter voltage of two BJT transistors with different collector currents has a positive TC. => **PTAT generator**
- Base currents are neglected => in practice, a beta correction circuit is needed.

General Block Diagram



$$V_{Ref} = V_{BE1} + \alpha\,\Delta V_{BE} = V_{BE1} + \alpha V_T \ln n$$

$$\Rightarrow \frac{\partial V_{Ref}}{\partial T} = \frac{\partial V_{BE1}}{\partial T} + \alpha\frac{\partial \Delta V_{BE}}{\partial T} = 0$$

$$\frac{\partial V_{BE}}{\partial T}\Big|_{T=300°K} \approx -1.5mV\ /°K, \quad V_{BE1} \approx 750\,mV$$

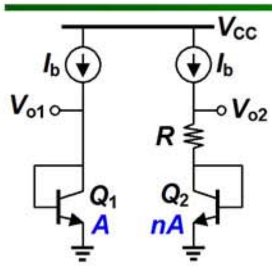
$$\frac{\partial \Delta V_{BE}}{\partial T}\Big|_{T=300°K} = \frac{k}{q} \approx 0.087mV\ /°K$$

$$\Rightarrow \alpha \ln n \approx 17.2$$

$$V_{Ref} \approx V_{BE1} + 17.2V_T \approx 1.2\,V$$

- Add PTAT and CTAT voltages with proper weights to achieve a zero TC.
- A temperature independent voltage reference is only realized at T = 300 °K.

Conceptual Scheme

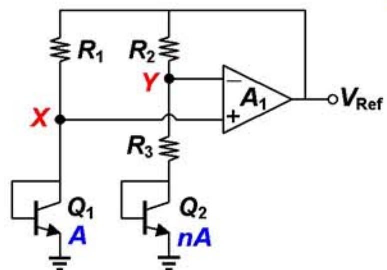


$$V_{o1} = V_{BE1}$$
$$V_{o2} = V_{BE2} + RI_b$$

$$V_{BE1} = V_{BE2} + RI_b$$
$$=> RI_b = V_{BE1} - V_{BE2}$$

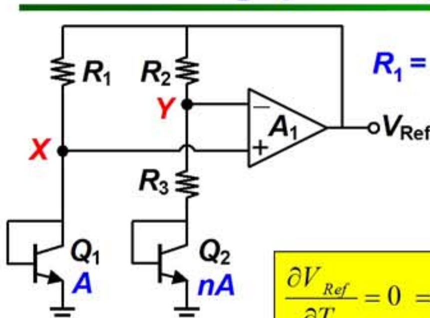
$$V_{o2} = V_{BE2} + V_{BE1} - V_{BE2} = V_{BE2} + V_T \ln n$$

Bandgap voltage



- Suppose V_{O1} and V_{O2} are somehow made equal.
- How do we make the V_{O1} and V_{O2} equal?
- How do we avoid $\ln n = 17.2$?
- Use an op-amp in negative feedback and a passive voltage divider.

Bandgap Voltage Reference Circuit



$R_1 = R_2$

$$I_{R3} = \frac{V_{BE1} - V_{BE2}}{R_3} = \frac{V_T \ln n}{R_3}$$

$$V_{Ref} = V_{BE2} + (R_2 + R_3) I_{R3} = V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) V_T \ln n$$

$$\frac{\partial V_{Ref}}{\partial T} = 0 \;=>\; \left(1 + \frac{R_2}{R_3}\right) \ln n \approx 17.2$$

$$n = 31,$$
$$R_1 = R_2 = 4R_3$$

An example

$$I_{C1} = I_{C2} \approx \frac{V_T \ln n}{R_3}$$

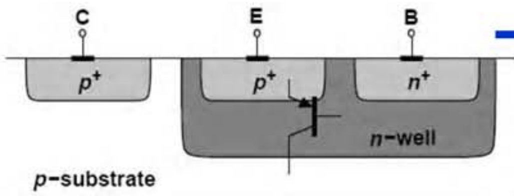
PTAT

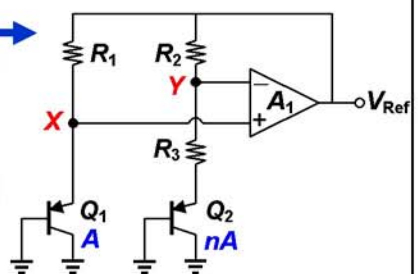
$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T}$$

- But, the collector current of both transistors is not temperature independent => changing TC of V_{BE}.
- In practice, accurate simulations are needed to estimate the TC of V_{BE}.

Compatibility with CMOS Technology

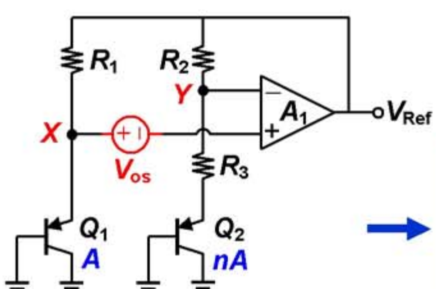
- Bipolar characteristics are essential here. Attempts at building purely CMOS precision references have not been very successful.
- How do we build this in CMOS?
- Called the lateral BJT has a small beta respected to the conventional vertical BJT transistors.
- Substrate is connected to the ground => collector is also connected to the GND.





Effect of Circuit Non-Idealities

- The op-amp non-idealities introduce various errors here. Let's consider the effect of offset.
- The op-amp offset voltage is multiplied by $(1+R_2/R_3)$.
- V_{OS} changes with temperature => increasing the overall TC.
- Note, the TC of resistors is not important!

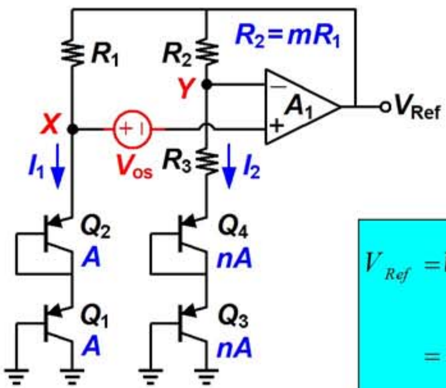


$$V_{EB1} - V_{OS} \approx V_{EB2} + R_3 I_{C2}$$
$$V_{Ref} = V_{EB2} + (R_2 + R_3) I_{C2}$$
$$R_1 = R_2, \quad I_{C1} \approx I_{C2}$$

$$V_{Ref} = V_{EB2} + (R_2 + R_3)\frac{V_{EB1} - V_{EB2} - V_{OS}}{R_3}$$
$$= V_{EB2} + \left(1 + \frac{R_2}{R_3}\right)(V_T \ln n - V_{OS})$$

Reducing the Effect of Op-Amp Offset Voltage

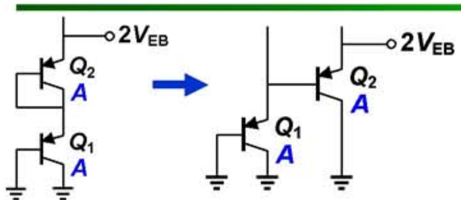
- Use of different currents and series connection of two diodes.
- But, the resulted reference voltage is about 2.5 V => its implementation is impossible in low supply voltages!
- This circuit cannot also be implemented in standard CMOS process.

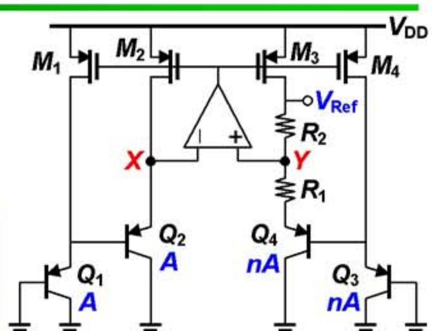


$$V_{EB1}+V_{EB2}-V_{OS}=V_{EB3}+V_{EB4}+R_3 I_2$$
$$V_{Ref}=V_{EB3}+V_{EB4}+\left(R_2+R_3\right)I_2$$
$$I_1\approx mI_2$$

$$V_{Ref}=V_{EB3}+V_{EB4}+\left(R_2+R_3\right)\frac{2V_T\ln\left(mn\right)-V_{OS}}{R_3}$$
$$=2V_{EB}+\left(1+\frac{R_2}{R_3}\right)\left[2V_T\ln\left(mn\right)-V_{OS}\right]$$

Modified Circuit

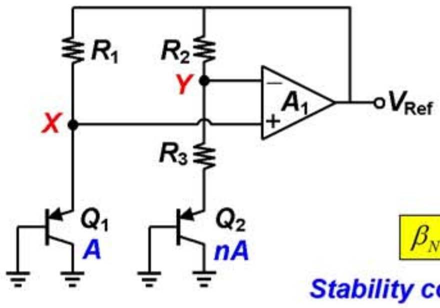




$$(W/L)_{1,2}=m\,(W/L)_{3,4}$$
$$V_{Ref}=V_{EB3}+V_{EB4}+\left(1+\frac{R_2}{R_1}\right)\times 2V_T\ln\left(mn\right)$$

- Op-amp adjusts the gate voltage of PMOS current source transistors so as to equalize V_X and V_Y.
- Op-amp is not loaded by the resistors.
- Mismatch between PMOS transistors makes an error in V_{Ref}.
- Channel length modulation in PMOS transistors increases the power supply sensitivity. => Use cascode current sources with long channel lengths.
- The limited beta of BJT transistors makes also an error in V_{Ref}. => needing a beta correction circuit.

Feedback Polarity



$$\beta_N = \frac{r_{e2}+R_3}{r_{e2}+R_3+R_2}$$

$$\beta_P = \frac{r_{e1}}{r_{e1}+R_1}, \quad r_{e1}=r_{e2}$$

$\beta_N > \beta_P$ → $\frac{r_{e2}+R_3}{r_{e2}+R_3+R_2} > \frac{r_{e1}}{r_{e1}+R_1}$

Stability condition

→ $R_1 R_3 > 0$

- There are two feedback networks here: one positive and one negative feedbacks!
- In practice, $\beta_N > 2\beta_P$ is considered to have a well behavior transient response with large capacitive loads!

Why It Is Called Bandgap?

$V_{Ref} = V_{BE} + V_T \ln n$ → $\frac{\partial V_{Ref}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{V_T}{T}\ln n = 0$

General form of a bandgap voltage

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

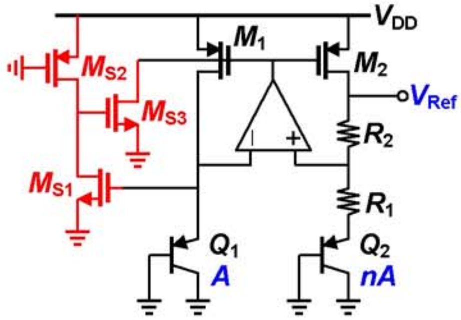
→ $V_{BE} + V_T \ln n = (4+m)V_T + E_g/q$

→ $V_{Ref} = (4+m)V_T + E_g/q$

$T \to 0 \;=>\; V_{Ref} \to E_g/q \approx 1.12V$

- So, V_{Ref} is called the bandgap reference voltage.

Supply Dependence and Start-Up



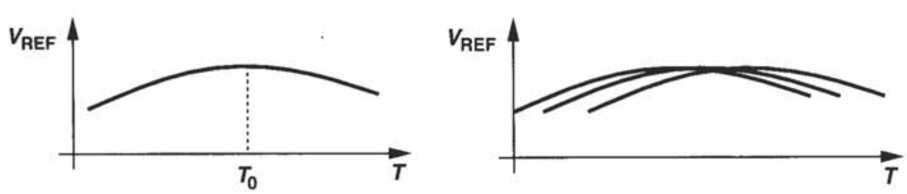
$$(W/L)_1 = m\,(W/L)_2$$

$$V_{Ref} = V_{EB2} + \left(1 + \frac{R_2}{R_1}\right) \times V_T \ln(mn)$$

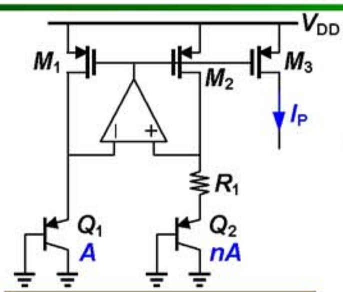
- A high dc gain amplifier is needed to achieve low sensitivity to V_{DD} variations => large PSRR.
- A start-up circuit is necessary to ensure non-zero current operating point during the circuit power on.

Curvature Correction

- TC of V_{Ref} is only zero at room temperature. In other temps, it is not zero due to second-order effects such as the amplifier offset voltage, V_{BE} TC changes, etc. => needs a curvature correction technique to achieve less than 20 ppm/°C TC.
- Samples of a bandgap reference displays substantially different zero-TC temperatures making it to correct the curvature reliably.
- A useful reference on curvature correction:
  - P. Malcovati et al., JSSC, July 2001.
  - This is the topic of ongoing active research.

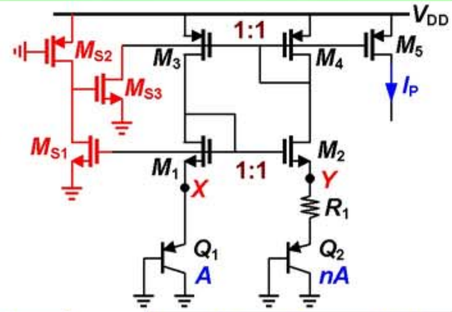


PTAT Current Generation



$$I_P = \frac{V_{EB1} - V_{EB2}}{R_1} = \frac{V_T \ln n}{R_1}$$

PTAT current

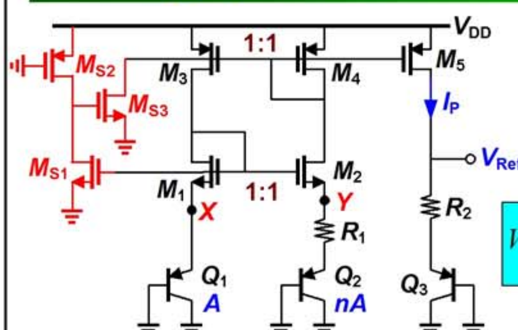


$$I_{D1} = I_{D2} \Rightarrow V_X = V_Y$$

$$I_P = \frac{V_{EB1} - V_{EB2}}{R_1} = \frac{V_T \ln n}{R_1}$$

- Assume identical PMOS transistors.
- It can also be used as a temperature sensor.
- We can use the constant-g_m biasing circuit to equalize V_X and V_Y without using an amplifier. => positive feedback
- In practice, the TC of resistor and mismatch between transistors changes the TC of I_P.

Bandgap Circuit with Constant-g_m Biasing

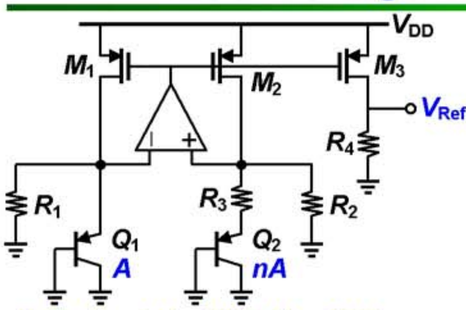


$$I_P = \frac{V_{EB1} - V_{EB2}}{R_1} = \frac{V_T \ln n}{R_1}$$

$$V_{Ref} = R_2 I_P + V_{EB3} = R_2 \frac{V_T \ln n}{R_1} + V_{EB3}$$

- Assume identical PMOS transistors.
- Low PSRR respected to when an op-amp is utilized.
- Use long channel length in current-mirror transistors or wide-swing cascode current mirrors to enhance the PSRR.

Low-Voltage Bandgap Circuit



H. Banba et al., JSSC, May 1999.

$$I_{R3} = \frac{V_{EB1} - V_{EB2}}{R_3} = \frac{V_T \ln n}{R_3}$$

PTAT current

$$R_1 = R_2 \Rightarrow I_{R2} = \frac{V_{EB1}}{R_2}$$

CTAT current

$$\rightarrow \quad I_{D3} = \frac{V_T \ln n}{R_3} + \frac{V_{EB1}}{R_2}$$

$$V_{Ref} = R_4 I_{D3} = \frac{R_4}{R_3} V_T \ln n + \frac{R_4}{R_2} V_{EB1}$$

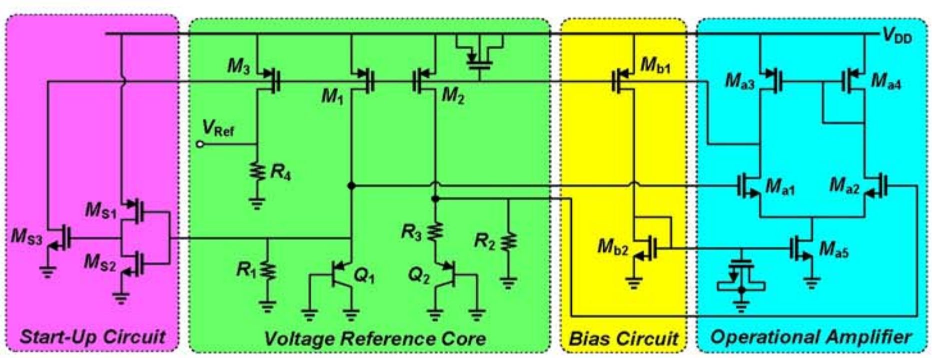
$$\frac{\partial V_{Ref}}{\partial T} = 0 \Rightarrow \frac{R_4}{R_3}\frac{V_T}{T}\ln n + \frac{R_4}{R_2}\frac{\partial V_{EB1}}{\partial T} = 0$$

$$\frac{\partial V_{BE}}{\partial T}\Big|_{T=300^\circ K} \approx -1.5mV/^\circ K,\ V_{BE1} \approx 750mV$$
$$R_1 = R_2 = 10k\Omega,\ R_3 = 2k\Omega = 2k\Omega,\ n = 31$$

$$\rightarrow \quad V_{Ref} = 239mV$$

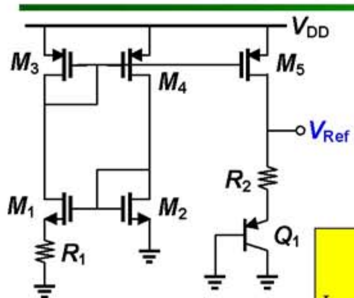
- How do generate a bandgap voltage less than 1.25 V?
- Assume identical PMOS transistors for simplicity.

Banba Bandgap Circuit Implementation



- A simple diff pair was used to realize the amplifier.
- The bias current generated by the bandgap core is used to bias the amplifier.
- It needs a start-up circuit.

MOS PTAT Current Generation



$$I_D = I_{D0}\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\times\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right]$$

MOS in weak inversion

$$R_1 I_{D1} + V_{GS1} = V_{GS2}, \quad \frac{I_{D1}}{I_{D2}} = \frac{(W/L)_3}{(W/L)_4}$$

$$I_{D1} = \frac{V_{GS2}-V_{GS1}}{R_1} = \frac{\eta V_T \ln\left(\frac{(W/L)_1}{(W/L)_2}\times\frac{(W/L)_4}{(W/L)_3}\right) + V_{TH2} - V_{TH1}}{R_1}$$

PTAT current

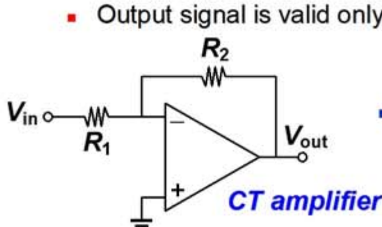
$$V_{Ref} = \frac{(W/L)_5}{(W/L)_3} I_{D1} R_2 + V_{EB1}$$

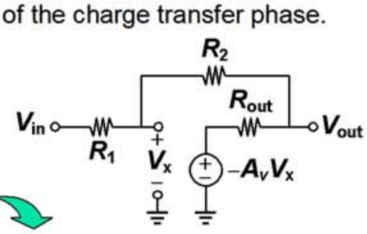
$$V_{Ref} = \frac{(W/L)_5}{(W/L)_3}\frac{R_2}{R_1}\eta V_T \ln\left(\frac{(W/L)_1}{(W/L)_2}\times\frac{(W/L)_4}{(W/L)_3}\right) + V_{EB1}$$ *Bandgap voltage*

- M_1 and M_2 are biased in the sub-threshold region.

Introduction

- **Continuous-time circuits**
  - High speed, low power, medium accuracy
  - Output signal is valid all the times.
- **Switched-capacitor circuits**
  - Medium speed, high accuracy
  - Output signal is valid only at the end of the charge transfer phase.





$$-A_v\left(\frac{V_{out}-V_{in}}{R_1+R_2}R_1 + V_{in}\right) - R_{out}\frac{V_{out}-V_{in}}{R_1+R_2} = V_{out}$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}\times\frac{A_v - R_{out}/R_2}{1+R_{out}/R_1 + A_v + R_2/R_1}$$

- Error in closed-loop gain due to large R_{out}.
- R_2 loads the amplifier and R_1 loads the previous stage amplifier => reducing A_v.